FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		TI-28234	
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT Jean-Louis Tardieux	
		FILING DATE October 1, 1999	GROUP

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE (IF APPROPRIATE)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION Yes	TRANSLATION No
SMD	BA	EP 0 649 085 A	4/19/95	Europe	G06F 9/38	—	X	
	BB							
	BC							
	BD							
	BE							
	BF							
	BG							

EXAMINER	DATE CONSIDERED
S. Deckter	03/04/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
	CA	TI-27677, *A Bit Field Processor*, co-filed as a regular application October 1, 1999.
	CB	TI-27678, *Rounding Mechanisms in Processors*, co-filed as a regular application October 1, 1999.
	CC	TI-27679, *Linear Vector Computation*, co-filed as a regular application October 1, 1999.
	CD	TI-27680, *Hardware Accelerator / Acceleration for Processing Systems*, co-filed as a regular application October 1, 1999.
	CE	TI-27681, *Pipeline Protection*, co-filed as a regular application October 1, 1999.
	CF	TI-27682, *Pipelined Hardware Stack*, co-filed as a regular application October 1, 1999.
	CG	TI-27683, *A Processor With Conditional Execution of an Instruction Pair*, co-filed as a regular application October 1, 1999.
	CH	TI-27684, *A Processor With Local Instruction Looping*, co-filed as a regular application October 1, 1999.
	CI	TI-27685, *Compound Memory Access Instructions*, co-filed as a regular application October 1, 1999.
	CJ	TI-27686, *A Processor With a Computed Repeat Instruction*, co-filed as a regular application October 1, 1999.
	CK	TI-27688, *A Processor With Apparatus for Verifying Instruction Parallelism*, co-filed as a regular application October 1, 1999.
	CL	TI-27689, *Cache Miss Benchmarking*, co-filed as a regular application October 1, 1999.
	CM	TI-27690, *A Processor With Apparatus for Indexed Branch During Instruction Iteration*, co-filed as a regular application October 1, 1999.
	CN	TI-27691, *Circular Buffer Management*, co-filed as a regular application October 1, 1999.
	CO	TI-27700, *Method and Apparatus for Accessing a Memory Core Multiple Times in a Single Clock Cycle*, co-filed as a regular application October 1, 1999.
	CP	TI-27757, *Improved Multiplier Accumulator Circuits*, co-filed as a regular application October 1, 1999.
	CQ	TI-27758, *Zero Anticipation Method and Apparatus*, co-filed as a regular application October 1, 1999.
	CR	TI-27759, *Trace FIFO Management*, co-filed as a regular application October 1, 1999.
	CS	TI-27760, *Stack Pointer Management*, co-filed as a regular application October 1, 1999.
	CT	TI-27761, *Software Breakpoint in a Delay Slot*, co-filed as a regular application October 1, 1999.
	CU	TI-27762, *Cache Coherence During Emulation*, co-filed as a regular application October 1, 1999.
	CV	TI-27763, *Memory Access Using Byte Qualifiers*, co-filed as a regular application October 1, 1999.
	CW	TI-27764, *Dual Interrupt Vector Mapping*, co-filed as a regular application October 1, 1999.
	CX	TI-28234, *Pipeline Protection*, co-filed as a regular application October 1, 1999.
	CY	TI-28433, *Improvements in or Relating to Microprocessors*, co-filed as a regular application October 1, 1999.
SMD	CZ	Paver, N.C., et al.; *Register Locking in an Asynchronous Microprocessor*, IEEE Proc. Of the Int'l Conf. On Computer Design: VL in Computers and Processors, Cambridge, MA, Oct. 11-14, 1992, pgs. 351-355.
SMD	DA	Shimamura, K., et al.; *A Superscalar RISC Processor With Pseudo Vector Processing Feature*, IEEE Int'l Conf. On Computer Design: VLSI in Computers and Processors, Austin, Oct. 2-4, 1995, pgs. 102-109.
SMD	DB	Kogge, P.; *The Architecture of Pipelined Computers*, 1981, Hemisphere Pub. Corp., Washington, US XP002096561, pgs. 220-225.

Not considered

EXAMINER	DATE CONSIDERED CZ-DB ONLY
S. Decker	03/04/02

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